

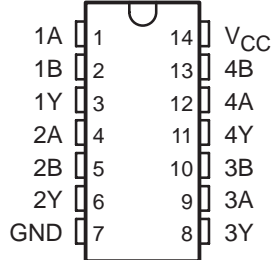
SN5400, SN54LS00, SN54S00 SN7400, SN74LS00, SN74S00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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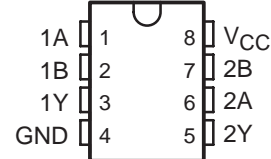
- Package Options Include Plastic Small-Outline (D, NS, PS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

- Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package

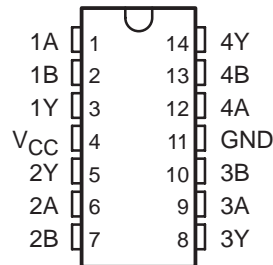
SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74S00 . . . D, N, OR NS PACKAGE
SN74LS00 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



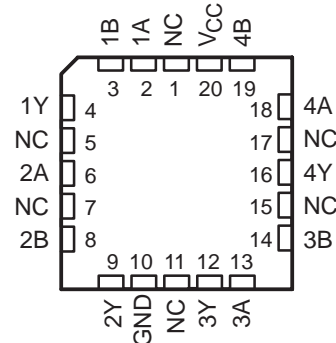
SN74LS00, SN74S00 . . . PS PACKAGE
(TOP VIEW)



SN5400 . . . W PACKAGE
(TOP VIEW)



SN54LS00, SN54S00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain four independent 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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description/ordering information (continued)

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|---------------|-----------------------|------------------|
| 0°C to 70°C | PDIP – N | Tube | SN7400N | SN7400N |
| | | | SN74LS00N | SN74LS00N |
| | | | SN74S00N | SN74S00N |
| | SOIC – D | Tube | SN7400D | 7400 |
| | | | SN7400DR | |
| | | Tape and reel | SN74LS00D | LS00 |
| | | | SN74LS00DR | |
| | | Tube | SN74S00D | S00 |
| | | | SN74S00DR | |
| | SOP – NS | Tape and reel | SN7400NSR | SN7400 |
| | | | SN74LS00NSR | 74LS00 |
| | | | SN74S00NSR | 74S00 |
| | SOP – PS | Tape and reel | SN74LS00PSR | LS00 |
| | | | SN74S00PSR | S00 |
| SSOP – DB | Tape and reel | SN74LS00DBR | LS00 | |
| –55°C to 125°C | CDIP – J | Tube | SNJ5400J | SNJ5400J |
| | | | SNJ54LS00J | SNJ54LS00J |
| | | | SNJ54S00J | SNJ54S00J |
| | CFP – W | Tube | SNJ5400W | SNJ5400W |
| | | | SNJ54LS00W | SNJ54LS00W |
| | | | SNJ54S00W | SNJ54S00W |
| | LCCC – FK | Tube | SNJ54LS00FK | SNJ54LS00FK |
| | | | SNJ54S00FK | SNJ54S00FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

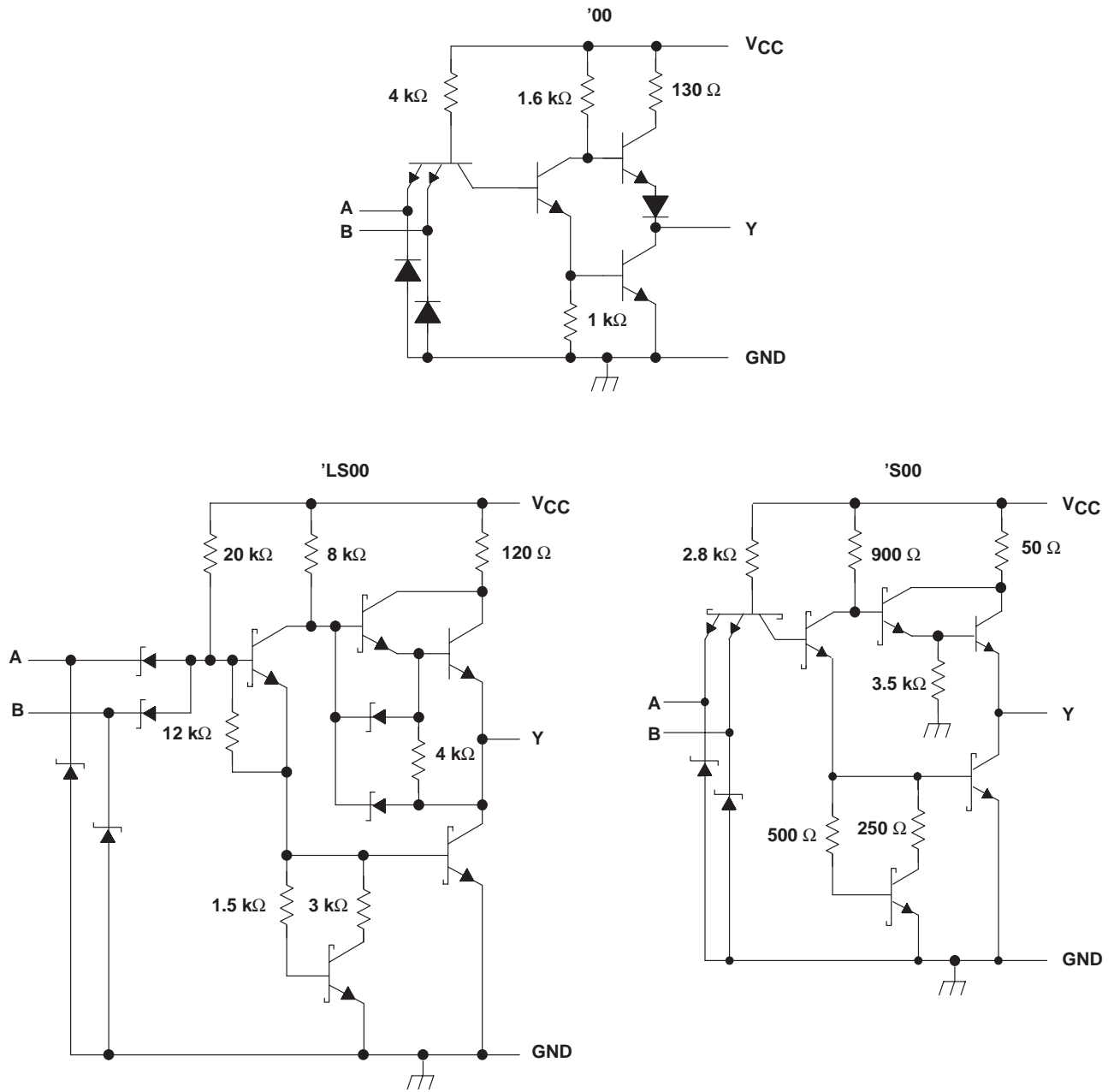
| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | L |
| L | X | H |
| X | L | H |

logic diagram, each gate (positive logic)



SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
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schematic



Resistor values shown are nominal.

**SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES**

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: '00, 'S00 | 5.5 V |
| 'LS00 | 7 V |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| DB package | 96°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| PS package | 95°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | SN5400 | | | SN7400 | | | UNIT |
|--------------------------------------|--------|-----|------|--------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} High-level output current | | | -0.4 | | | -0.4 | mA |
| I_{OL} Low-level output current | | | 16 | | | 16 | mA |
| T_A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | SN5400 | | | SN7400 | | | UNIT |
|---------------------------|---|--------|------|------|--------|------|------|------|
| | | MIN | TYP§ | MAX | MIN | TYP§ | MAX | |
| V_{IK} | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} | $V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$ | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| V_{OL} | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$ | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I_I | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | 1 | | | 1 | mA |
| I_{IH} | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$ | | | 40 | | | 40 | µA |
| I_{IL} | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | | | -1.6 | | | -1.6 | mA |
| $I_{OS}^{\dagger\dagger}$ | $V_{CC} = \text{MAX}$ | -20 | | -55 | -18 | | -55 | mA |
| I_{CCH} | $V_{CC} = \text{MAX}, V_I = 0 \text{ V}$ | | 4 | 8 | | 4 | 8 | mA |
| I_{CCL} | $V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$ | | 12 | 22 | | 12 | 22 | mA |

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

†† Not more than one output should be shorted at a time.



SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN5400 SN7400 | | | UNIT |
|-----------|--------------|-------------|--|------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | |
| t_{PLH} | A or B | Y | $R_L = 400\ \Omega$, $C_L = 15\text{ pF}$ | | 11 | 22 | ns |
| t_{PHL} | | | | | 7 | 15 | |

recommended operating conditions (see Note 4)

| | SN54LS00 | | | SN74LS00 | | | UNIT |
|--------------------------------------|----------|-----|------|----------|-----|------|------------------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} High-level output current | | | -0.4 | | | -0.4 | mA |
| I_{OL} Low-level output current | | | 4 | | | 8 | mA |
| T_A Operating free-air temperature | -55 | | 125 | 0 | | 70 | $^\circ\text{C}$ |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS [†] | SN54LS00 | | | SN74LS00 | | | UNIT |
|---------------|---|------------------------|------------------|------|----------|------------------|------|---------------|
| | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| V_{IK} | $V_{CC} = \text{MIN}$, $I_I = -18\text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} | $V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $I_{OH} = -0.4\text{ mA}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V_{OL} | $V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$ | $I_{OL} = 4\text{ mA}$ | | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | $I_{OL} = 8\text{ mA}$ | | | | 0.35 | 0.5 | |
| I_I | $V_{CC} = \text{MAX}$, $V_I = 7\text{ V}$ | | | 0.1 | | | 0.1 | mA |
| I_{IH} | $V_{CC} = \text{MAX}$, $V_I = 2.7\text{ V}$ | | | 20 | | | 20 | μA |
| I_{IL} | $V_{CC} = \text{MAX}$, $V_I = 0.4\text{ V}$ | | | -0.4 | | | -0.4 | mA |
| I_{OS}^{\S} | $V_{CC} = \text{MAX}$ | -20 | | -100 | -20 | | -100 | mA |
| I_{CCH} | $V_{CC} = \text{MAX}$, $V_I = 0\text{ V}$ | | 0.8 | 1.6 | | 0.8 | 1.6 | mA |
| I_{CCL} | $V_{CC} = \text{MAX}$, $V_I = 4.5\text{ V}$ | | 2.4 | 4.4 | | 2.4 | 4.4 | mA |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN54LS00 SN74LS00 | | | UNIT |
|-----------|--------------|-------------|---|----------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | |
| t_{PLH} | A or B | Y | $R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$ | | 9 | 15 | ns |
| t_{PHL} | | | | | 10 | 15 | |



SN5400, SN54LS00, SN54S00
SN7400, SN74LS00, SN74S00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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recommended operating conditions (see Note 5)

| | | SN54S00 | | | SN74S00 | | | UNIT |
|-----------------|--------------------------------|---------|-----|-----|---------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | | 0.8 | | | V |
| I _{OH} | High-level output current | | | | -1 | | | mA |
| I _{OL} | Low-level output current | | | | 20 | | | mA |
| T _A | Operating free-air temperature | -55 | | | 125 | | | °C |

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54S00 | | | SN74S00 | | | UNIT |
|-------------------|---|---------|------|------|---------|------|------|------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IK} | V _{CC} = MIN, I _I = -18 mA | -1.2 | | | -1.2 | | | V |
| V _{OH} | V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -1 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 20 mA | 0.5 | | | 0.5 | | | V |
| I _I | V _{CC} = MAX, V _I = 5.5 V | 1 | | | 1 | | | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | 50 | | | 50 | | | µA |
| I _{IL} | V _{CC} = MAX, V _I = 0.5V | -2 | | | -2 | | | mA |
| I _{OS} § | V _{CC} = MAX | -40 | | -100 | -40 | | -100 | mA |
| I _{CCH} | V _{CC} = MAX, V _I = 0 V | 10 16 | | | 10 16 | | | mA |
| I _{CCL} | V _{CC} = MAX, V _I = 4.5 V | 20 36 | | | 20 36 | | | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

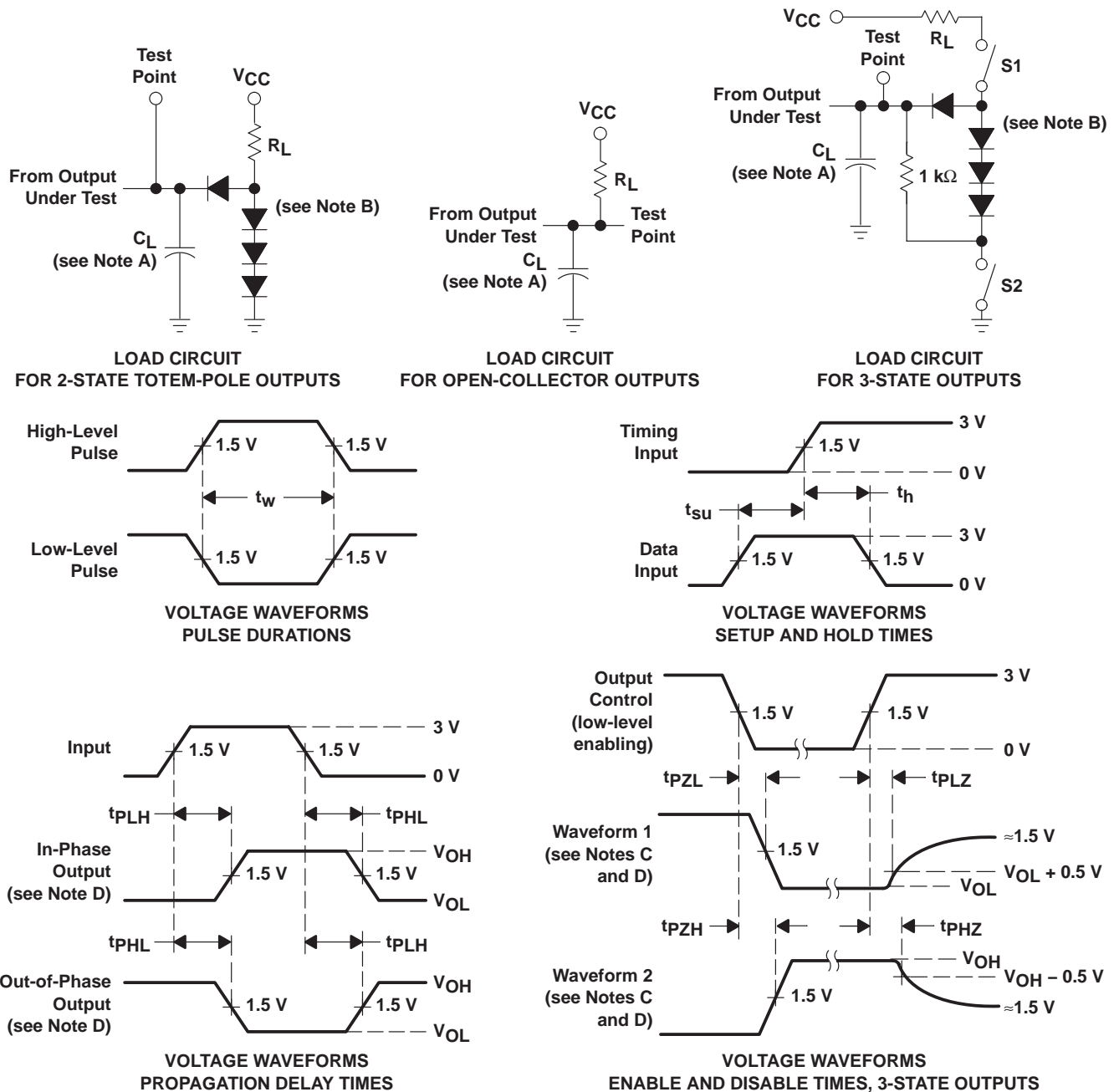
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN54S00 SN74S00 | | | UNIT |
|------------------|--------------|-------------|--|--------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | |
| t _{PLH} | A or B | Y | R _L = 280 Ω, C _L = 15 pF | 3 4.5 | | | ns |
| t _{PHL} | | | | 3 5 | | | |
| t _{PLH} | A or B | Y | R _L = 280 Ω, C _L = 50 pF | 4.5 | | | ns |
| t _{PHL} | | | | 5 | | | |



PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| JM38510/00104BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| JM38510/00104BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| JM38510/07001BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| JM38510/07001BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| JM38510/30001B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| JM38510/30001BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| JM38510/30001BDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| JM38510/30001SCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| JM38510/30001SDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN5400J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN54LS00J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN54S00J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN7400D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN7400DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN7400DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN7400DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN7400DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN7400DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN7400N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN7400N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN7400NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN7400NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN7400NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN7400NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00DBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI |
| SN74LS00DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00DBRE4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00DBRG4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| | | | | | | no Sb/Br) | | |
| SN74LS00DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00J | OBSOLETE | CDIP | J | 14 | | TBD | Call TI | Call TI |
| SN74LS00N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS00NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS00NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00PSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00PSRE4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS00PSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74S00N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN74S00NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74S00NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00NSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00PSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00PSRE4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74S00PSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SNJ5400J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ5400W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ5400WA | OBSOLETE | CFP | WA | 14 | | TBD | A42 | N / A for Pkg Type |
| SNJ54LS00FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54LS00J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54LS00W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54S00FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54S00J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54S00W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



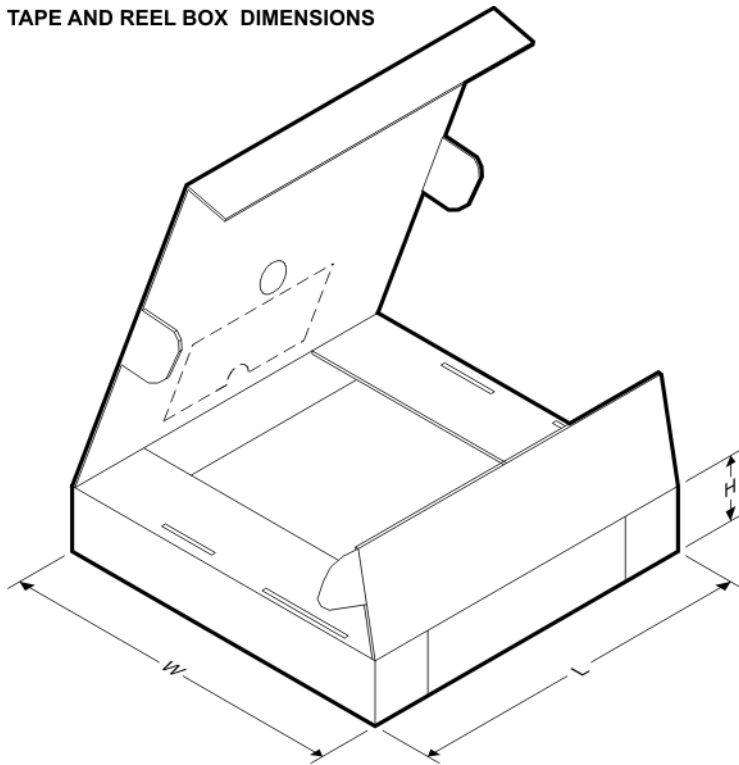
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN7400DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN7400NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS00DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS00DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS00NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS00PSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74S00DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74S00NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74S00PSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN7400DR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| SN7400NSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LS00DBR | SSOP | DB | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LS00DR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| SN74LS00NSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LS00PSR | SO | PS | 8 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74S00DR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| SN74S00NSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74S00PSR | SO | PS | 8 | 2000 | 346.0 | 346.0 | 33.0 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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